

项目名称: P60-X9 V6.0

开案日期: 2012.8.14

开案规格:

VST59S with TSUMV59S

全功能版本: 名称 料号

规格

公板版本: 名称 料号

规格

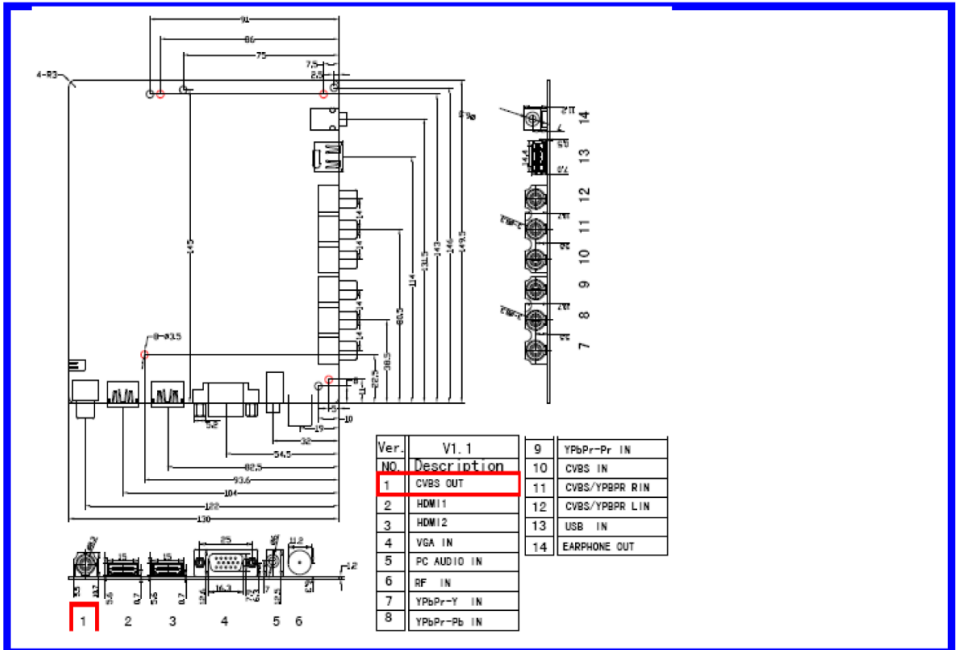
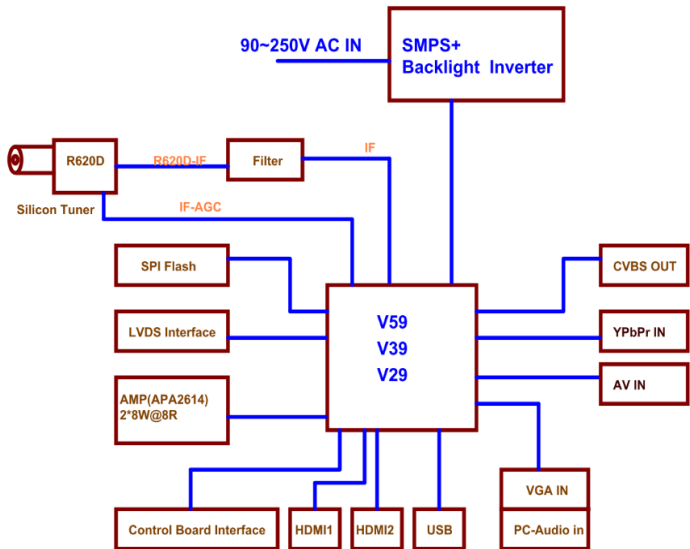
版本更新记录

| 版本 | 更新记录 | 修订 | 审核 | 日期 |
|----------------------|---|----------|----|------------|
| P60-X9 V6.1 20130117 | 在P60-x9 v6.0-B 基础上修改电源部分为48V+12V,板卡这边删除19V to12 DC/DC 并增加12V switch及修改功放供电及Mute电路, 将之功放供电电容由一个改为两个。 | suncheng | | 2013.01.17 |
| | | | | |
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| | | | | |

Power Config:



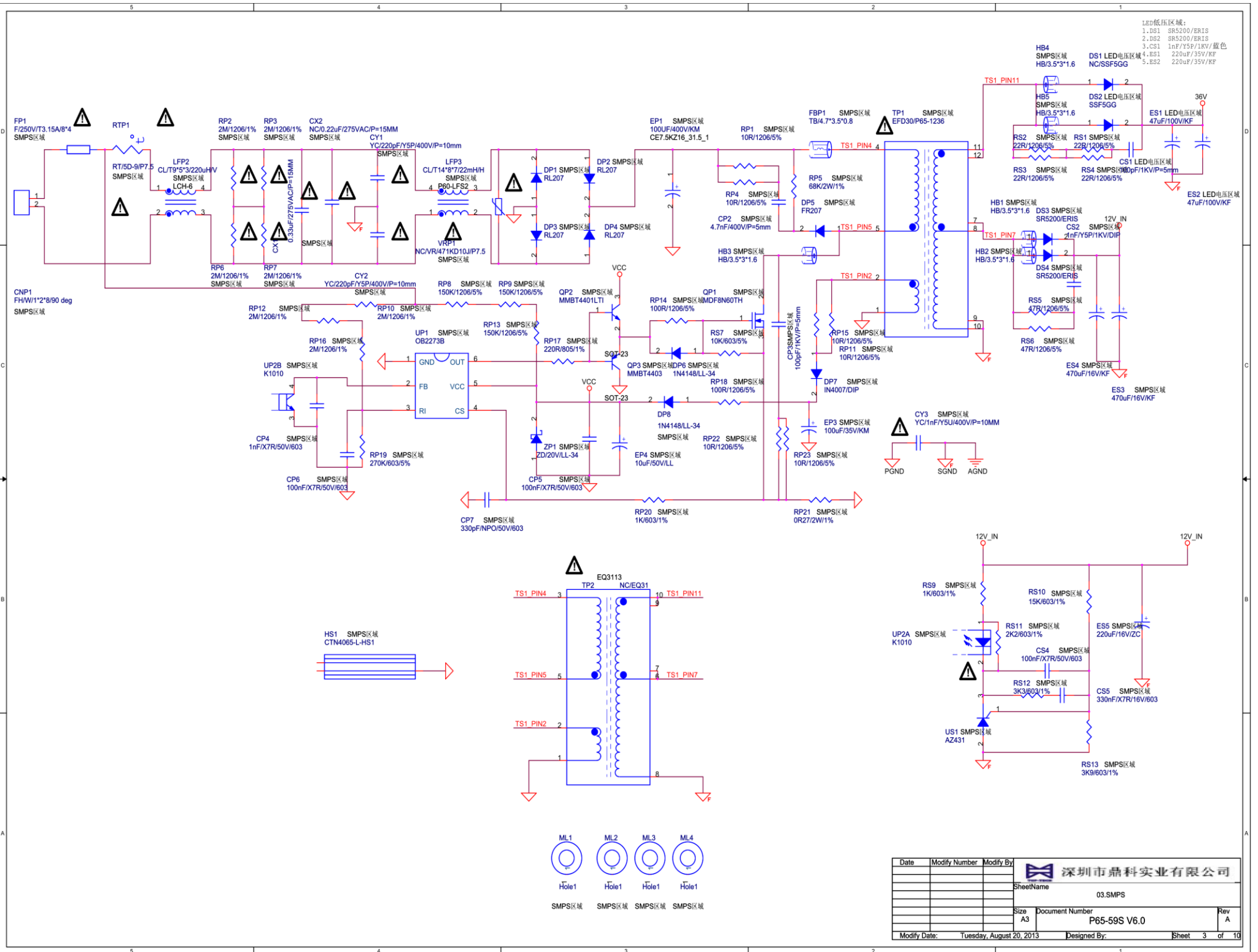
Block diagram



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|--------------|-------------------------|--------------|-------------|-----------------------------|
| | | | SheetName | 01.Page Cover |
| | | | Size A3 | Document Number P6-59S V6.0 |
| | | | Rev A | |
| Modify Date: | Monday, August 19, 2013 | Designed By: | suncheng | Sheet 1 of 10 |

GPIO CONFIG

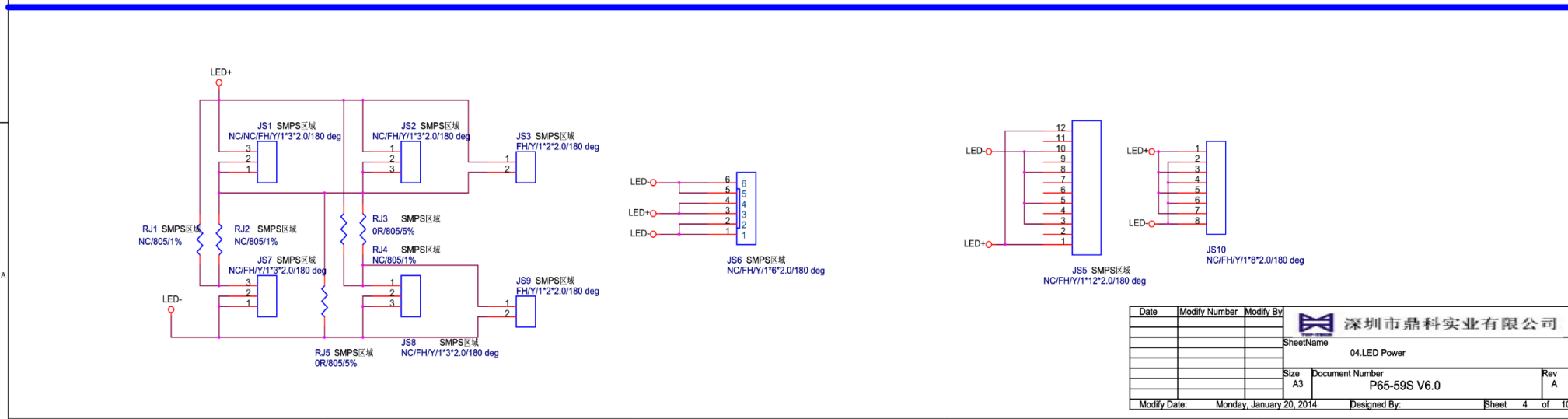
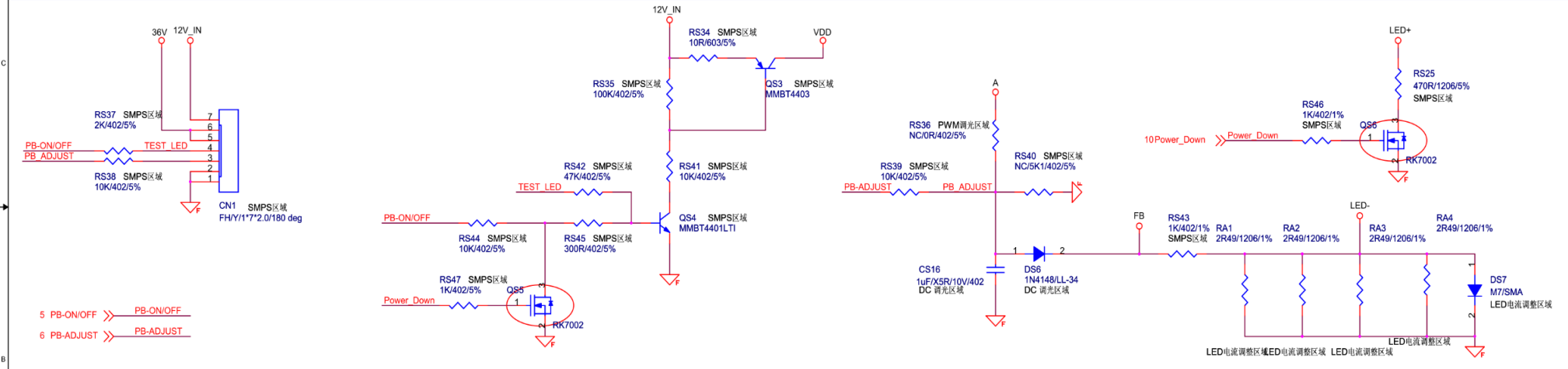
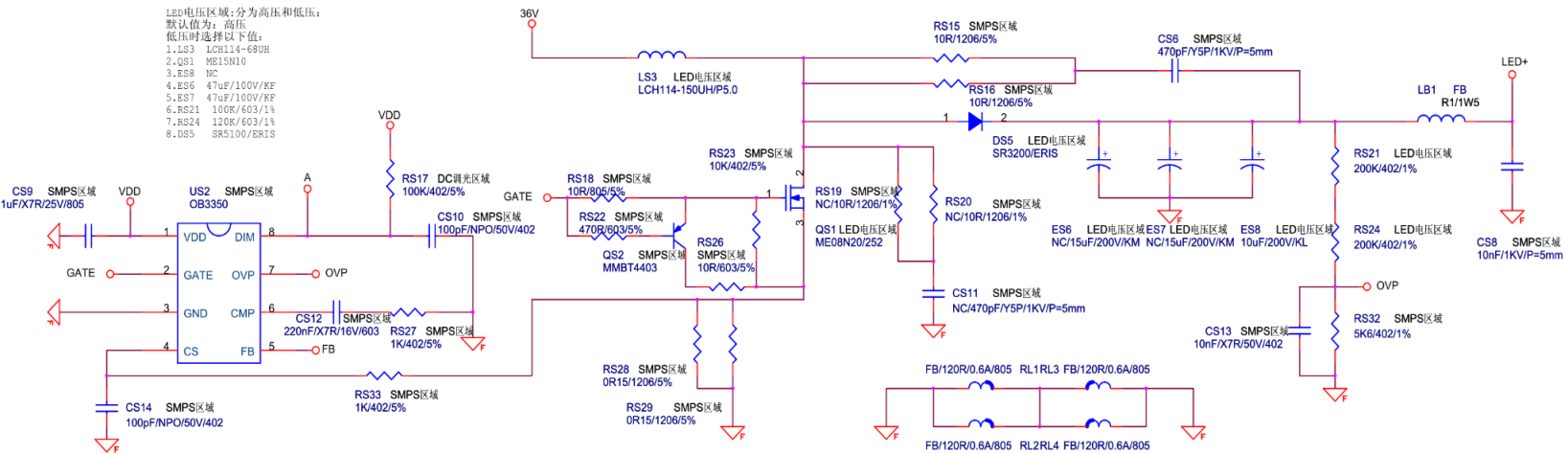
| Pin Number | Pin Name | Net Name | Functional Description | Control State | Remarks |
|------------|---------------|-----------------|--|---|-----------------------------------|
| 70 | INT | PWR-ON/OFF | 电源待机控制 | H:Power ON L:Standby | 同公板一样 |
| 44 | GPIO2 | PANEL_ON/OFF | 屏供电控制 | H: ON L:OFF | 同公板一样 |
| 71 | TCNO0 | VBL_CTRL | 屏背光开关控制 | H:OFF L:ON | 同公板一样 |
| 79 | PWM0 | BRI_ADJ-PWM0 | 屏背光调节控制脚 | 有两个方式: 1.PWM 调光 2.DC调光 | 同公板一样 |
| 86 | IRIN | IRIN | 遥控信号输入 | | 同公板一样 |
| 84 | SAR0 | KEY0-SAR0 | AD按键输入 | 一线7键式AD按键 | 同公板一样 |
| 85 | URP_TEST/SAR1 | SAR1 | LED控制口 | H:LED RED L:LED Green | 这个口同时还控制功放MUTE H:LED RED 同时功放MUTE |
| 30/31 | AUOUTL/R0 | AMP-AUOUTR0 | 功放Audio 输入 | | |
| 32/33 | AUOUTL/R1 | ADUO_OUT_L | AV out Audio 输出 | | |
| 19 | CVBS0 | AV1-Vin | AV1 CVBS 输入 | | |
| 18 | CVBS1 | AV2-Vin | AV2 CVBS 输入 | | |
| 21 | CVBSOUT | CVBS_OUT | AV OUT CVBS 输出 | | |
| 26/27 | AUL/R4 | AV1-L/Rin | AV1 Audio R/L 输入 | | |
| 28/29 | AUL/R5 | AV2-L/Rin | AV2 Audio R/L 输入 | | |
| 23/24 | AUL/R0 | VGA_L/R | VGA Audio R/L 输入 | | |
| 6 | GIN0P | RGB0_Y+ | VGA Y信号输入 | | |
| 5 | SOGIN0 | RGB0_Y-SOG | VGA 同步信号输入 (兼容老式机器) | | |
| 4 | BIN0P | RGB0_Pb+ | VGA Pb信号输入 | | |
| 8 | RIN0P | RGB0_Pr+ | VGA Pr信号输入 | | |
| 9 | VSYNC0 | VGA_VS | VGA 场同步信号输入 | | |
| 3 | HSYNC0 | VGA_HS | VGA 行同步信号信号输入 | | |
| 11 | BIN1P | RGB2-HDTV_BIN | YPbPr接口 Pb信号输入 | | |
| 12 | SOGIN1 | RGB2-HDTV_SOGIN | YPbPr接口 同步信号输入 | | |
| 13 | GIN1P | RGB2-HDTV_GIN | YPbPr接口 Y信号输入 | | |
| 15 | RIN1P | RGB2-HDTV_RIN | YPbPr接口 Pr信号输入 | | |
| 16 | AVDD_33 | Scart_FB | 选TSUMV59芯片时, SCART FB信号输入 | 1-3V RGB 0-0.4V:CVBS | |
| 85 | URP_TEST/SAR1 | Scart_FS | 选TSUMV59芯片时, SCART FS信号输入 | 2.02-2.55V: 4:3 1.06-1.70V :16:9 0-0.43:无信号 (这是指scart信号经过10K和2.7K电阻分压后CPU检测的电压值) | |
| 49 | VLACKP | RXEC+/LED_CTR | 选TSUMV59芯片时, LVDS CLK 采用1推二的方式, 因此这个空出来作LED控制脚 | H:LED RED L:LED Green | 这个口同时还控制功放MUTE H:LED RED 同时功放MUTE |
| 50 | VLACKM | RXEC-/5V330_CTR | 选TSUMV59芯片时, LVDS CLK 采用1推二的方式, 当有scart功能时这个作5V330控制脚, | L:SCART H:YPbPr_IN | |



LED低压区域:
 1. DS1 SR5200/ER1S
 2. DS2 SR5200/ER1S
 3. CS1 1nF/25F/1KV/蓝色
 4. ES1 220uF/35V/KF
 5. ES2 220uF/35V/KF

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| SheetName | | |
| 03.SMPS | | |
| Size | | Document Number |
| A3 | | P65-59S V6.0 |
| Modify Date: | | Designed By: |
| Tuesday, August 20, 2013 | | Sheet 3 of 10 |

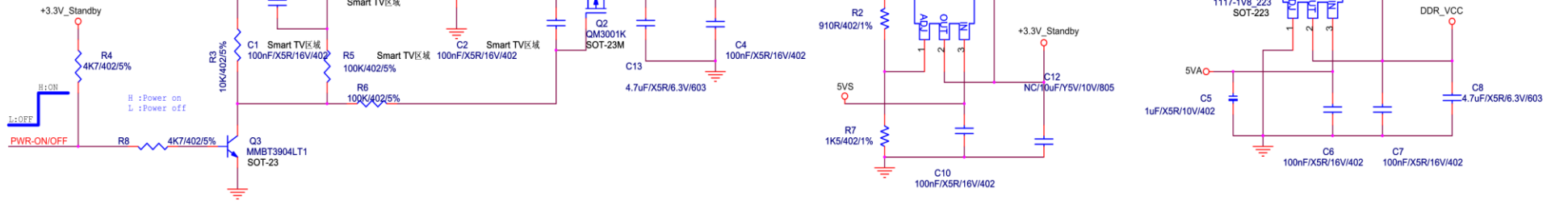
LED电压区域:分为高压和低压:
默认值为: 高压
低值时选择以下值:
1.LS3 LCH114-68UH
2.QS1 ME15N10
3.E68 NC
4.E66 47uF/100V/KF
5.E67 47uF/100V/KF
6.RS21 100K/402/1%
7.RS24 120K/603/1%
8.DS5 SR5100/ERIS



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|--------------|--------------------------|--------------|------------------------|------------------------------|-------|
| | | | SheetName 04.LED Power | | |
| | | | Size A3 | Document Number P65-59S V6.0 | Rev A |
| Modify Date: | Monday, January 20, 2014 | Designed By: | Sheet 4 of 10 | | |

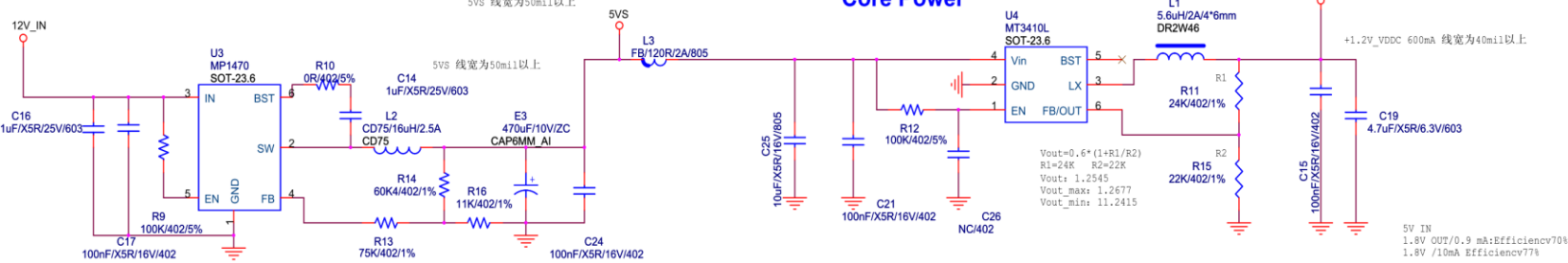
Power Input

Standby controller



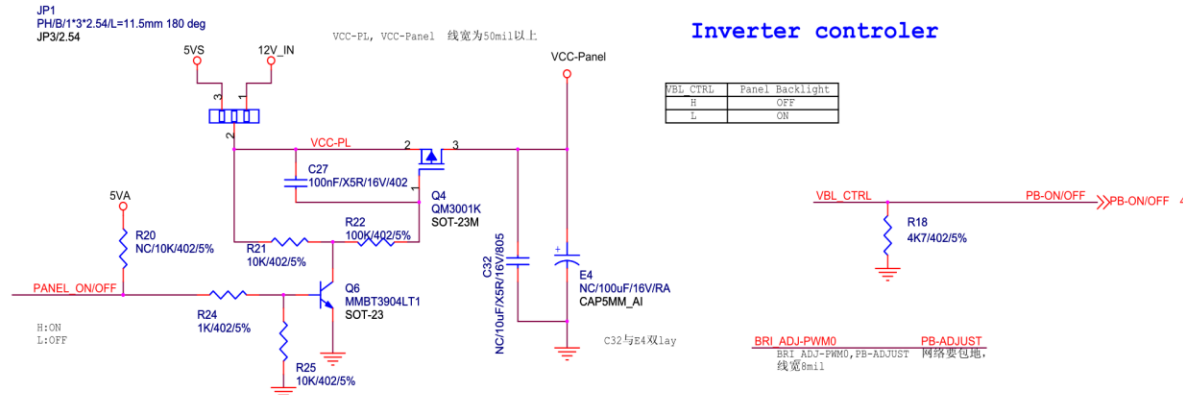
System Power

Core Power

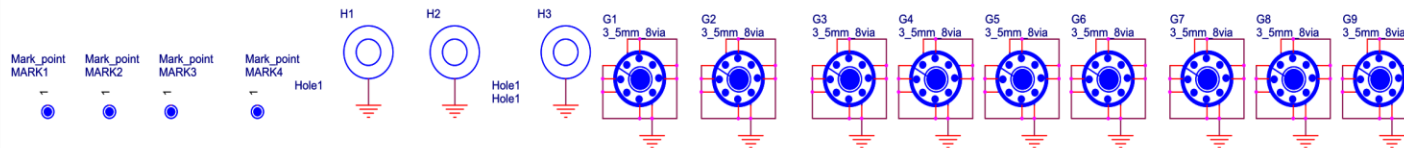


PANEL POWER

Inverter controller

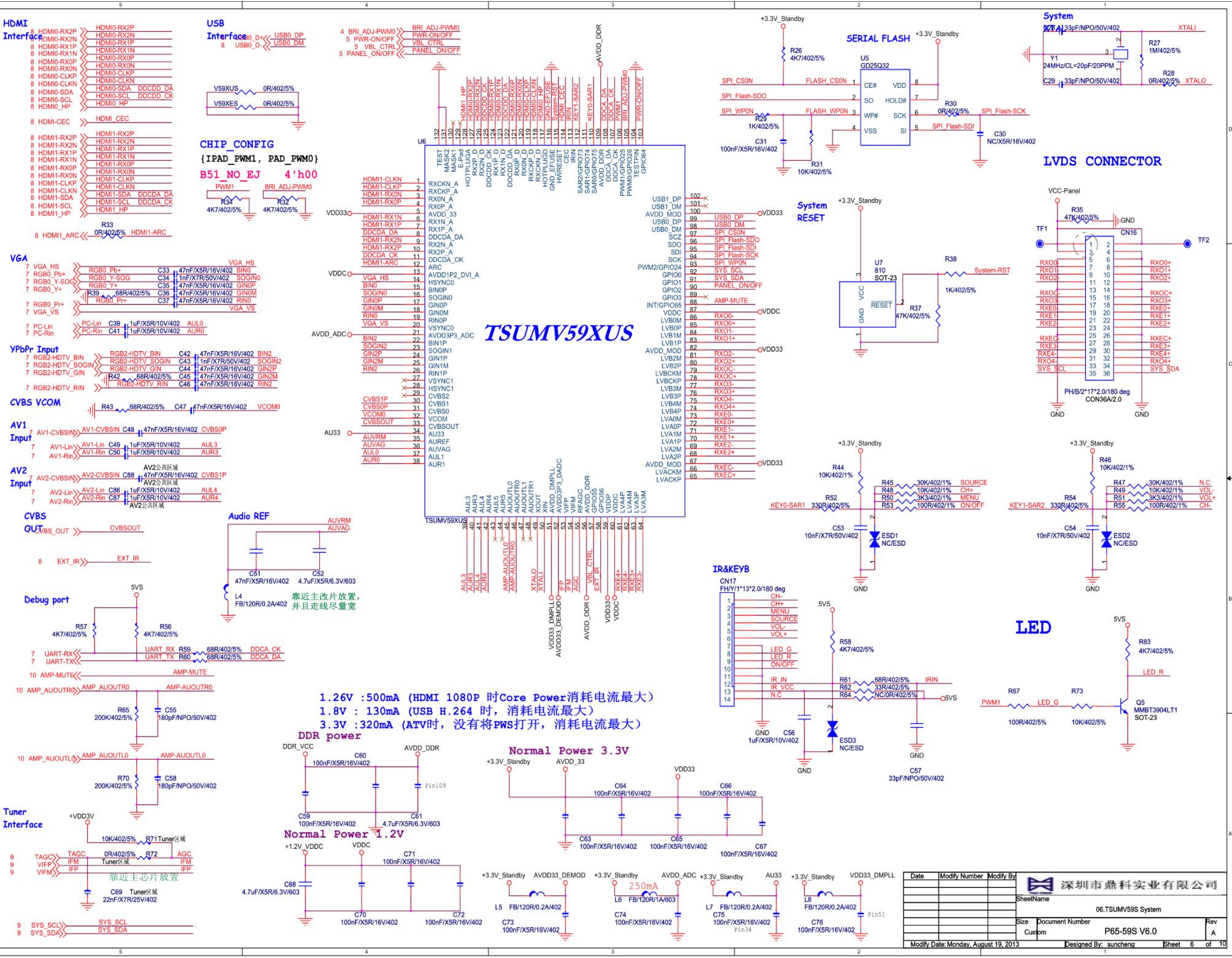


- VBL_CTRL << VBL_CTRL 6
- BRI_ADJ-PWM0 << BRI_ADJ-PWM0 4.6
- PANEL_ON/OFF << PANEL_ON/OFF 6
- PWR-ON/OFF << PWR-ON/OFF 6
- PB-ADJUST >> PB-ADJUST 4.6



| Date | Modify Number | Modify By | SheetName | Size | Document Number | Rev |
|--------------|-------------------------|--------------|-----------------|---------------|-----------------|-----|
| | | | 05.System Power | A3 | P65-59S V6.0 | A |
| Modify Date: | Monday, August 19, 2013 | Designed By: | suncheng | Sheet 5 of 19 | | |

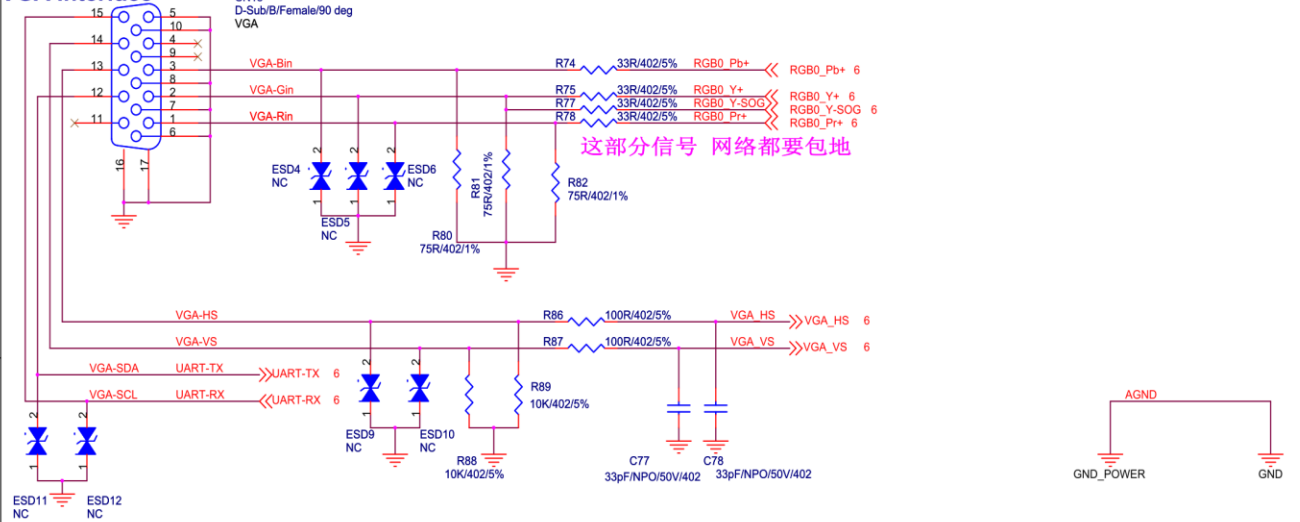
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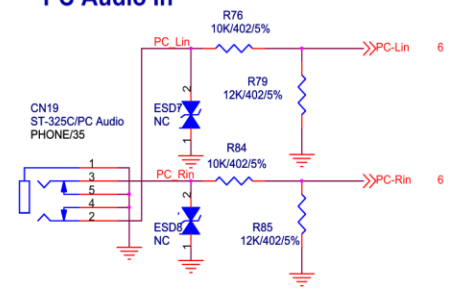
| Date | Modify Number | Modify By |
|------|---------------|-----------|
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 SheetName: 06.TSUMV59S System
 Size: Cuspm
 Document Number: P65-59S V6.0
 Rev: A
 Modify Date: Monday, August 19, 2013
 Designed by: suncheng
 Sheet 6 of 10

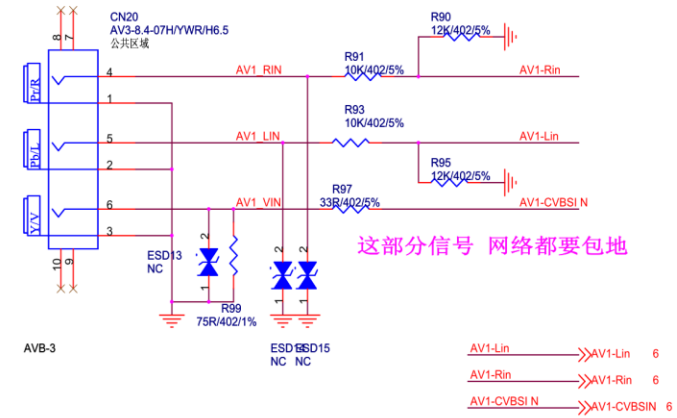
VGA Interface



PC Audio In



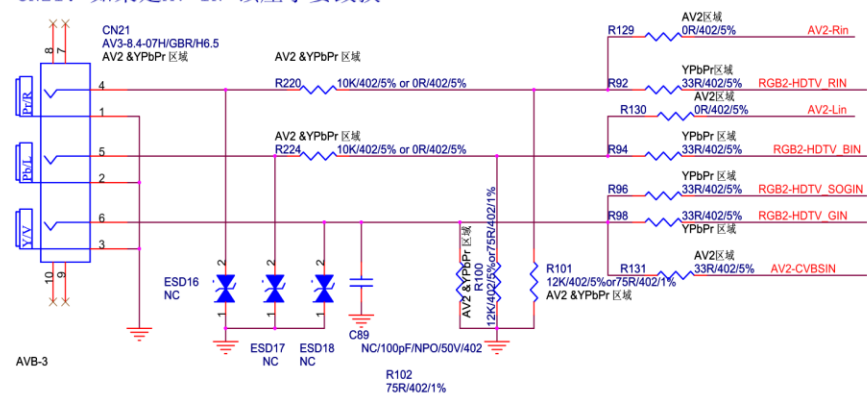
AV Interface



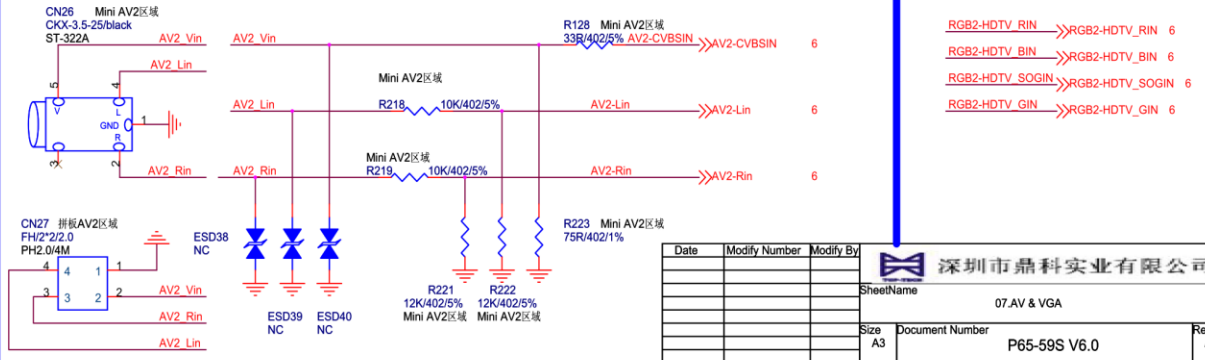
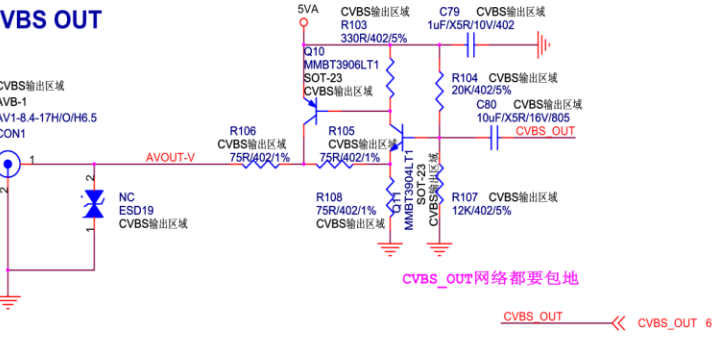
YPBPR_IN Interface

CN21: 如果是AV IN 该座子要改换

这部分信号 网络都要包地



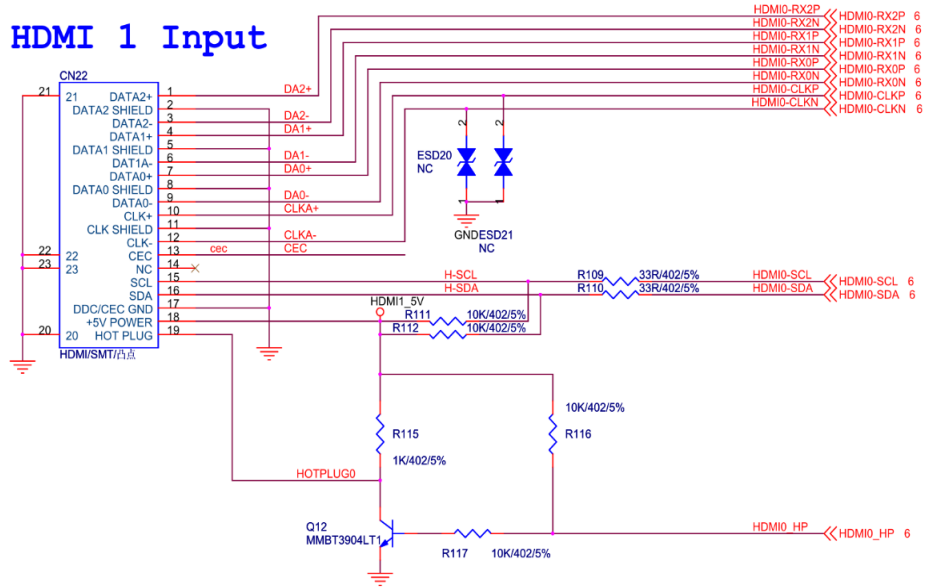
CVBS OUT



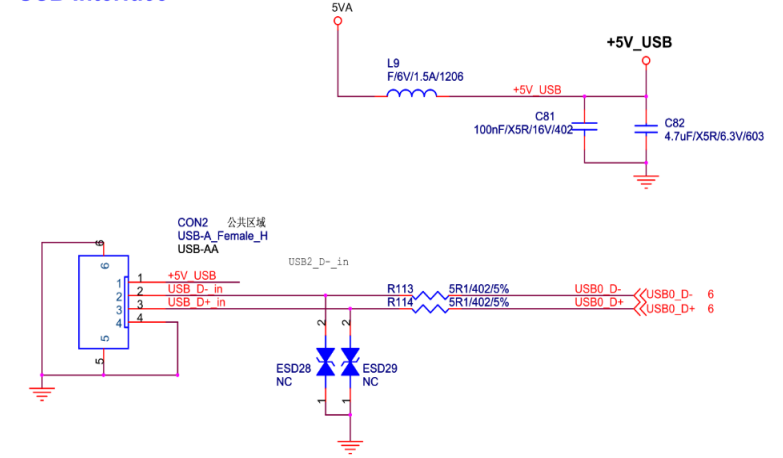
| Date | Modify Number | Modify By |
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 SheetName: 07 AV & VGA
 Size: A3
 Document Number: P65-59S V6.0
 Rev: A
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 Designed By: sunchena
 Sheet: 7 of 10

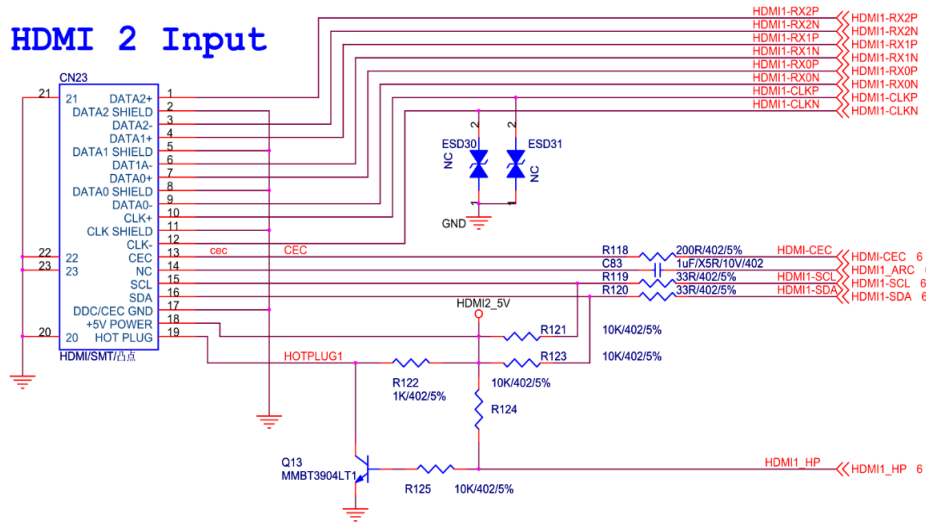
HDMI 1 Input



USB Interface



HDMI 2 Input



外甩座子和HDMI1座子双lay

SMART TV INTERFACE

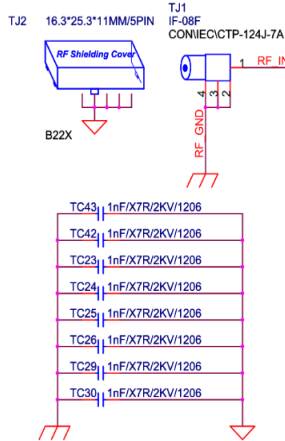


| Date | Modify Number | Modify By | SheetName | Size | Document Number | Rev |
|--------------|--------------------------|--------------|---------------|-------|-----------------|-------|
| | | | 08.HDMI & USB | A3 | P65-59S V6.0 | A |
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Silicon Tuner:R620D

RF GND与JAGND的安全间距要求大于1.2mm
两个屏蔽罩之间也要1.2mm



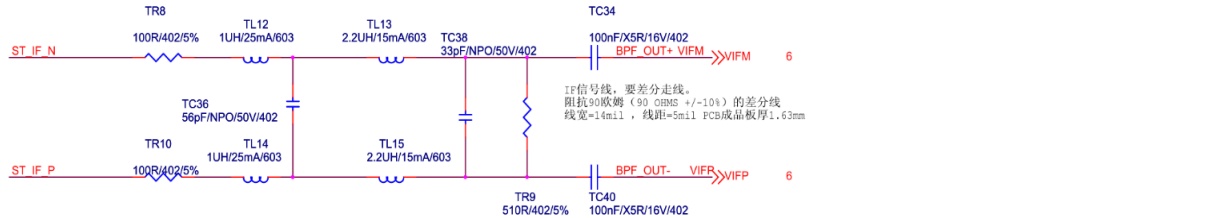
RF 信号输入部分走线，要走75欧姆的阻抗线。
即线径为20mil，走线与GND的间距为17mil。PCB成品板厚1.63mm

M01:
U9 PCB footprint 改为
MCL601RF-10 QFN24P_050_025_400X，
同S1S的一种。
20121120

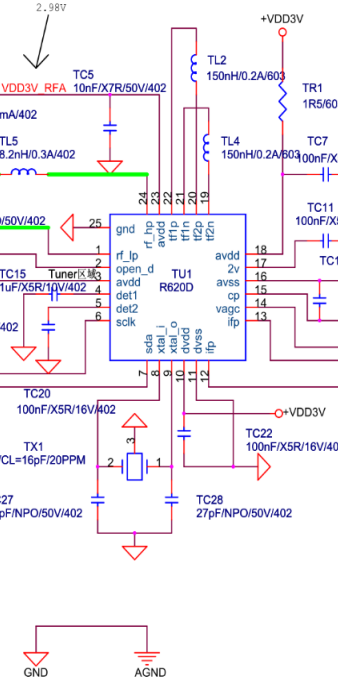
| | C114 | C115 | L16 | L17 | C123 | C124 |
|----------------------|------|------|-------|-------|-------|-------|
| Add Notch filter | 68pF | 47pF | 220nH | 220nH | 120pF | 150pF |
| Not Add Notch filter | 10nF | 10nF | NC | NC | NC | NC |

M01:
1>.L8由0R改为5R6/402/5%
2>.C120由2.2uF/603/35V改为1uF
3>.C125由56pF改为100pF.
4>.删除R177,R179,R178
---20120213

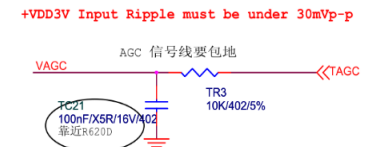
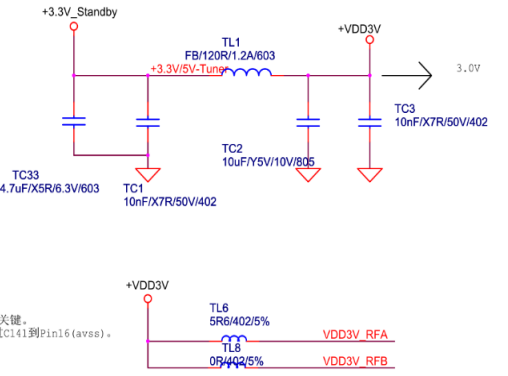
C137=180P, FOR 38.9MHZ OR 38MHZ (PAL)
C137=100P, FOR 45.75MHZ (NTSC)



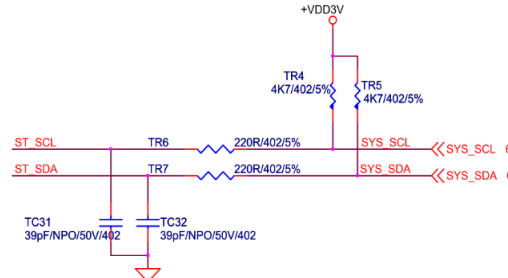
IF信号线，要差分走线。
阻抗90欧姆（90 OHMS +/-10%）的差分线
线宽=14mil，线距=5mil PCB成品板厚1.63mm



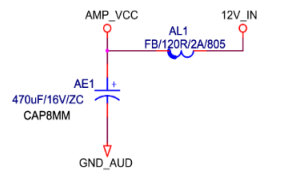
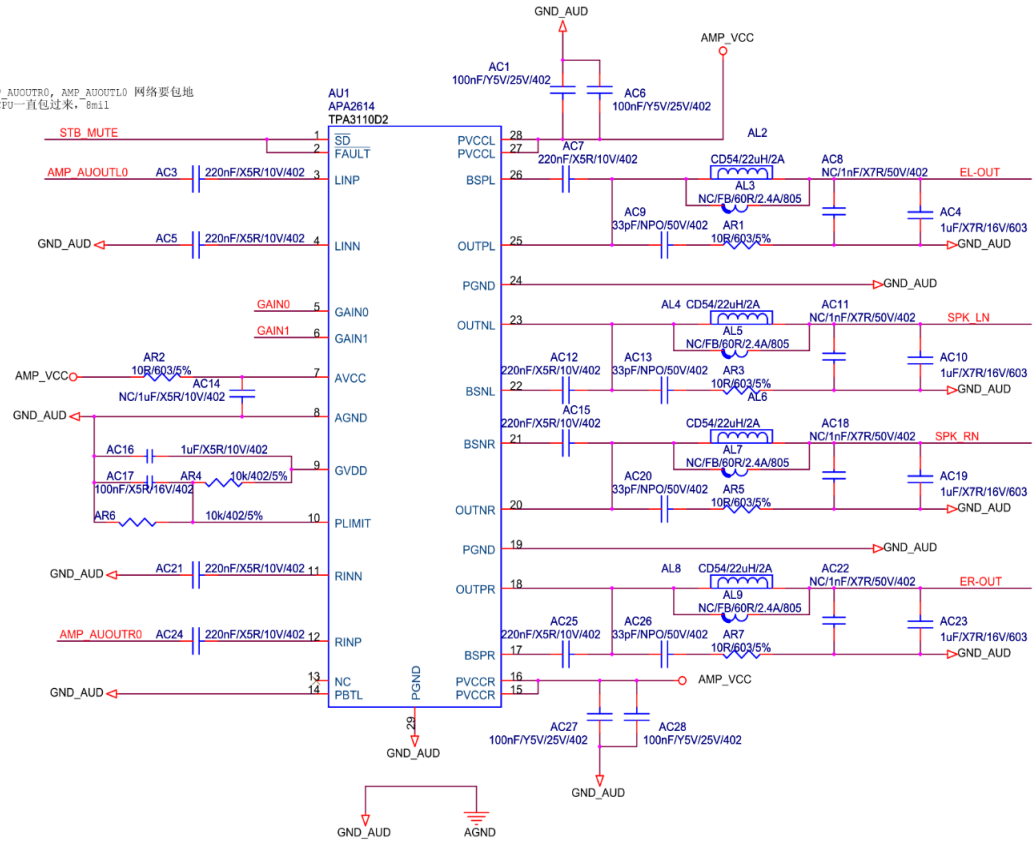
IF信号线，要差分走线。
阻抗90欧姆（90 OHMS +/-10%）的差分线
线宽=14mil，线距=5mil PCB成品板厚1.63mm



+VDD3V Input Ripple must be under 30mVp-p

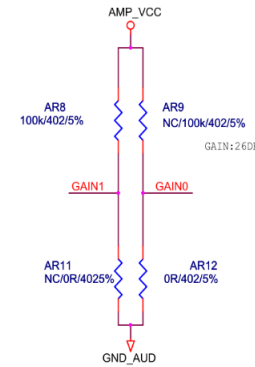
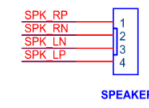


AMP_AUOUTR0, AMP_AUOUTL0 网络要包地
从CFU一直包过来, 6m11

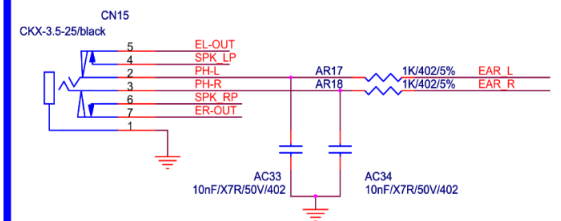
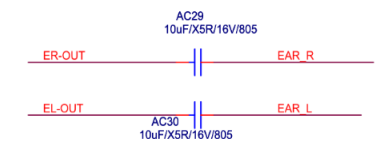
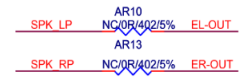


功效输出走线要求在40m11 以上

ACN1
FH/Y/1*4*2.54/180 deg
CON4/2.54



EARPHONE OUT



- Power_Down >>> Power_Down
- AMP_AUOUTL0 <<< AMP_AUOUTL0 6
- AMP_AUOUTR0 <<< AMP_AUOUTR0 6
- AMP-MUTE <<< AMP-MUTE 6

| GAIN1 | GAIN0 | AMPLIFIER GAIN (dB) | | INPUT IMPEDANCE (kΩ) | |
|-------|-------|---------------------|-----|----------------------|-----|
| | | TYP | TYP | TYP | TYP |
| 0 | 0 | 20 | 60 | | |
| 0 | 1 | 26 | 30 | | |
| 1 | 0 | 32 | 15 | | |
| 1 | 1 | 36 | 9 | | |

| NAME | Pin # | I/O/P | DESCRIPTION |
|-------|-------|-------|--|
| SD | 1 | I | Shutdown logic input for audio amp (LOW = outputs Hi-Z, HIGH = outputs enabled). TTL logic levels with compliance to AVCC. |
| FAULT | 2 | O | Open drain output used to display short circuit or dc detect fault status. Voltage compliant to AVCC. Short circuit faults can be set to auto-recovery by connecting FAULT pin to SD pin. Otherwise, both short circuit faults and dc detect faults must be reset by cycling PVCC. |
| GAIN0 | 5 | I | Gain select least significant bit. TTL logic levels with compliance to AVCC. |
| GAIN1 | 6 | I | Gain select most significant bit. TTL logic levels with compliance to AVCC. |

| | | | | |
|--------------|--------------------------|--------------|-------------|-----------------|
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| | | | SheetName | 10_Amplify |
| | | | Size | Document Number |
| | | | A3 | P65-59S V6.0 |
| Modify Date: | Tuesday, August 20, 2013 | Designed By: | suncheng | Sheet 10 of 10 |